In the claims:

Claim 42 (previously presented) An integrated circuit having a plurality of I/O modules, comprising:

a substrate;

a bond pad disposed on said substrate;

an electrostatic discharge device disposed in the substrate, the electrostatic discharge device being at least partially disposed beneath the bond pad;

circuitry disposed in said substrate;

an I/O buffer disposed in the substrate and connected to the bond pad for providing communication between the bond pad and said circuitry, said circuitry positioned substantially adjacent to both the electrostatic discharge device and the I/O buffer.

Claim 43 (previously presented) The integrated circuit of claim 42 wherein the substrate is a silicon substrate.

Claim 44 (previously presented) The integrated circuit of claim 42 wherein the I/O buffer is an output buffer.

Claim 45 (previously presented) The integrated circuit of claim 42 wherein the I/O buffer is an input buffer.

Claim 46 (previously presented) The integrated circuit of claim 42 wherein the I/O buffer is a complementary output buffer.

Claim 47 (previously presented) The integrated circuit of claim 42 wherein the circuitry is CMOS circuitry.

Claim 48 (previously presented) The integrated circuit of claim 42 wherein the circuitry is BiCMOS circuitry.

Claim 49 (previously presented) The integrated circuit of claim 42 wherein the circuitry is an application specific integrated circuit.

Claim 50 (previously presented) The integrated circuit of claim 42 wherein the circuitry is digital signal processor.

Claim 51 (previously presented) The integrated circuit of claim 42 wherein the entire surface of the substrate beneath the bond pad is occupied by the electrostatic discharge device.

Claim 52 (withdrawn) A semiconductor wafer which comprises:

a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by a scribe region at the periphery of each said integrated circuit; each of said integrated circuits including:

a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device; and

an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region..

Claim 53 (withdrawn) A semiconductor wafer which comprises:

a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by a scribe region at the periphery of each said integrated circuit; each of said integrated circuits including:

a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device disposed at least partially beneath said bond pad; and

an I/O buffer disposed between said scribe region and said core region.

Claim 54 (withdrawn) The semiconductor wafer of claim 53 wherein said I/O buffer is further disposed laterally of said bond pad relative to said core region and said scribe region.

Claim 55 (withdrawn) An integrated circuit which comprises:

a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device; and

an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region..

Claim 56 (withdrawn) An integrated circuit which comprises:

a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device disposed at least partially beneath said bond pad; and

an I/O buffer disposed between said scribe region and said core region.

Claim 57 (withdrawn) The circuit of claim 56 wherein said I/O buffer is further disposed laterally of said bond pad relative to said core region and said scribe region.

Claim58 (withdrawn).A method of fabricating a semiconductor wafer which comprises the steps of:

providing a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by a scribe region at the periphery of each said integrated circuit; and providing in each of said integrated circuits:

a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device; and

an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region..

Claim 59 (withdrawn) A method of fabricating a semiconductor wafer which comprises the steps of:

providing a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by a scribe region at the periphery of each said integrated circuit; and providing in each of said integrated circuits:

a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device disposed at least partially beneath said bond pad; and

an I/O buffer disposed between said scribe region and said core region.

Claim 60 (withdrawn) The method of claim 59 wherein said I/O buffer is further disposed laterally of said bond pad relative to said core region and said scribe region.

Claim 61 (withdrawn) A method of fabricating an integrated circuit which comprises the steps of:

providing a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

providing at least one bond pad disposed between said core region and said scribe region;

providing an electrostatic discharge device; and

providing an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region..

Claim 62 (withdrawn) A method of fabricating an integrated circuit which comprises the steps of:

providing a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

providing at least one bond pad disposed between said core region and said scribe region;

providing an electrostatic discharge device disposed at least partially beneath said bond pad; and

providing an I/O buffer disposed between said scribe region and said core region.

Claim 63 (withdrawn) The method of claim 62 wherein said I/O buffer is further disposed laterally of said bond pad relative to said core region and said scribe region.